19-2543; Rev 0; 7/02

MAXIM

Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs

General Description

The MAX9317/MAX9317A/MAX9317B/MAX9317C low-skew, dual 1-to-5 differential drivers are designed for clock and data distribution. The differential input is reproduced at five LVDS outputs with a low output-to-output skew of 5ps.

The MAX9317/MAX9317A are designed for low-voltage operation from a 2.375V to 2.625V power supply for use in 2.5V systems. The MAX9317B/MAX9317C operate from a 3.0V to 3.6V power supply for use in 3.3V systems. The MAX9317A/MAX9317C feature 50Ω input termination resistors to reduce component count.

The MAX9317 family is available in 32-pin 7mm × 7mm TQFP and space-saving 5mm × 5mm QFN packages and operate across the extended temperature range of -40°C to +85°C. The MAX9317A is pin compatible with ON Semiconductor's MC100EP210S.

Applications

Precision Clock Distribution

Low-Jitter Data Repeaters

Data and Clock Drivers and Buffers

Central-Office Backplane Clock Distribution

DSLAM Backplanes

Base Stations

ATE

Pin Configurations appear at end of data sheet.

Features

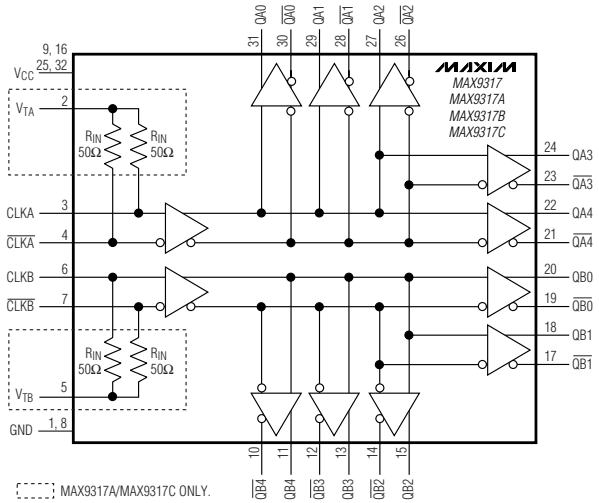
- **Guaranteed 1.0GHz Operating Frequency**
- **145ps (max) Part-to-Part Skew**
- **5ps Output-to-Output Skew**
- **330ps Propagation Delay from CLK_ to Q_**
- **2.375V to 2.625V Operation (MAX9317/MAX9317A)**
- **3.0V to 3.6V Operation (MAX9317B/MAX9317C)**
- **ESD Protection: ±2kV (Human Body Model)**
- **Internal 50Ω Input Termination Resistors (MAX9317A/MAX9317C)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	NOMINAL SUPPLY VOLTAGE (V)
MAX9317ETJ*	-40°C to +85°C	32 Thin QFN	2.5
MAX9317ECJ	-40°C to +85°C	32 TQFP	2.5
MAX9317AETJ*	-40°C to +85°C	32 Thin QFN	2.5
MAX9317AECJ	-40°C to +85°C	32 TQFP	2.5
MAX9317BETJ*	-40°C to +85°C	32 Thin QFN	3.3
MAX9317BECJ	-40°C to +85°C	32 TQFP	3.3
MAX9317CETJ*	-40°C to +85°C	32 Thin QFN	3.3
MAX9317CECJ	-40°C to +85°C	32 TQFP	3.3

**Future product—contact factory for availability.*

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.1V
Input Pins to GND.....-0.3V to (V_{CC} + 0.3V)
Differential Input Voltage .....V_{CC} or 3.0V, whichever is less
Continuous Output Current.....28mA
Surge Output Current.....50mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin, 7mm × 7mm TQFP
(derate 20.7mW/°C above +70°C).....1.65W
32-Pin 5mm × 5mm QFN
(derate 21.3mW/°C above +70°C).....1.7W

Junction-to-Ambient Thermal Resistance in Still Air
32-Pin, 7mm × 7mm TQFP.....+48.4°C/W
32-Pin, 5mm × 5mm QFN .....+47°C/W
Junction-to-Case Thermal Resistance
32-Pin, 7mm × 7mm TQFP.....+12°C/W
32-Pin, 5mm × 5mm QFN .....+2°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (CLK_, $\overline{CLK_}$, Q_, $\overline{Q_}$, $V_{T_}$) .....±2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.375V to 2.625V (MAX9317/MAX9317A), V_{CC} = 3.0V to 3.6V (MAX9317B/MAX9317C), all outputs loaded 100Ω ±1% between Q_ and $\overline{Q_}$, unless otherwise noted. Typical values are at V_{CC} = 2.5V (MAX9317/MAX9317A), V_{CC} = 3.3V (MAX9317B/MAX9317C), $V_{IHD} = V_{CC}$ - 1.0V, $V_{ILD} = V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		-40°C			+25°C			+85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUTS (CLK_, $\overline{CLK_}$)													
Differential Input High Voltage	V_{IHD}	Figure 1		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 1		0		V_{CC} - 0.1	0		V_{CC} - 0.1	0		V_{CC} - 0.1	V
Differential Input Voltage	V_{ID}	V_{IHD} - V_{ILD}	MAX9317/ MAX9317A	0.1		V_{CC}	0.1		V_{CC}	0.1		V_{CC}	V
			MAX9317B/ MAX9317C	0.1		3.0	0.1		3.0	0.1		3.0	
Input Current	I_{IH}, I_{IL}	CLK_, or $\overline{CLK_}$ = V_{IHD} or V_{ILD}, MAX9317/MAX9317B		-60		+60	-60		+60	-60		+60	µA
Input Termination Resistance	R_{IN}	MAX9317A/MAX9317C, Figure 2 (Note 4)		43	50	57	43	50	57	43	50	57	Ω
OUTPUTS (Q_, $\overline{Q_}$)													
Output High Voltage	V_{OH}	Figure 1				1.6			1.6			1.6	V
Output Low Voltage	V_{OL}	Figure 1		0.9			0.9			0.9			V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.375V to 2.625V (MAX9317/MAX9317A), V_{CC} = 3.0V to 3.6V (MAX9317B/MAX9317C), all outputs loaded 100Ω ±1% between Q_ and $\overline{Q}$_, unless otherwise noted. Typical values are at V_{CC} = 2.5V (MAX9317/MAX9317A), V_{CC} = 3.3V (MAX9317B/MAX9317C), $V_{IHD} = V_{CC}$ - 1.0V, $V_{ILD} = V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Output Voltage	V_{OD}	Figure 1	250	350	450	250	350	450	250	350	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}			7	50		6	50		6	50	mV
Output Offset Voltage	V_{OS}		1.125	1.25	1.375	1.125	1.25	1.375	1.125	1.25	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}				25			25			25	mV
Output Short-Circuit Current	I_{OSC}	Q_ shorted to $\overline{Q_}$			12			12			12	mA
		Q_ or $\overline{Q_}$ shorted to GND			28			28			28	
POWER SUPPLY												
Power-Supply Current (Note 5)	I_{CC}	MAX9317/9317A		69	107		75	107		80	107	mA
		MAX9317B/9317C		75	107		81	107		86	107	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.375V to 2.625V (MAX9317/MAX9317A) or V_{CC} = 3.0V to 3.6V (MAX9317B/MAX9317C), all outputs loaded with 100Ω ±1%, between Q_ and $\overline{Q}$_, $f_{IN} \le$ 1.0GHz, input transition time = 125ps (20% to 80%), $V_{IHD} - V_{ILD}$ = 0.15V to V_{CC}, unless otherwise noted. Typical values are at V_{CC} = 2.5V (MAX9317/MAX9317A), V_{CC} = 3.3V (MAX9317B/MAX9317C), f_{IN} = 1.0GHz, $V_{IHD} = V_{CC}$ - 1.0V, $V_{ILD} = V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1 and 4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay CLK_, $\overline{CLK_}$ to Q_, $\overline{Q_}$	t_{PHL} t_{PLH}	Figure 1	250	310	600	250	330	600	250	335	600	ps
Output-to-Output Skew	t_{SKEW1}	(Note 6)		9	55		5	45		4	25	ps
Part-to-Part Skew	t_{SKEW2}	(Note 7)			145			145			145	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.0GHz, clock pattern (Note 8)		0.8	2.0		0.8	2.0		0.8	2.0	$ps_{(RMS)}$
Added Deterministic Jitter	t_{DJ}	f_{IN} = 1.0GHz, 2^{23} - 1 PRBS pattern (Note 8)		80	105		80	105		80	105	$ps_{(P-P)}$
Operating Frequency	f_{MAX}	$V_{OD} \ge$ 250mV	1.0			1.0			1.0			GHz

Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.375V to 2.625V (MAX9317/MAX9317A) or V_{CC} = 3.0V to 3.6V (MAX9317B/MAX9317C), all outputs loaded with 100Ω ±1%, between Q_ and $\overline{Q}$_, $f_{IN} \le$ 1.0GHz, input transition time = 125ps (20% to 80%), V_{IHD} - V_{ILD} = 0.15V to V_{CC}, unless otherwise noted. Typical values are at V_{CC} = 2.5V (MAX9317/MAX9317A), V_{CC} = 3.3V (MAX9317B/MAX9317C), f_{IN} = 1.0GHz, V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1 and 4)

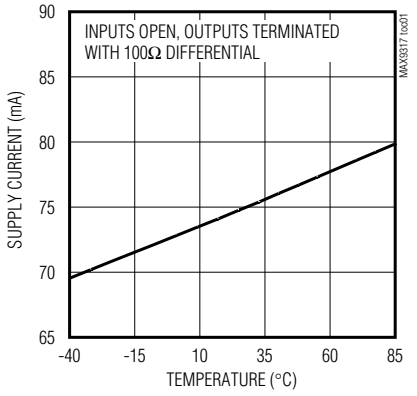
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Output Rise/Fall Time	t_R/t_F	20% to 80%, Figure 1	140	200	300	140	205	300	140	205	300	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: Guaranteed by design and characterization, and are not production tested. Limits are set to ±6 sigma.
Note 5: All outputs loaded with 100Ω differential, all inputs biased differential high or low except $V_{T_}$.
Note 6: Measured between outputs of the same device at the signal crossing points for a same-edge transition.
Note 7: Measured between outputs on different devices for identical transitions and V_{CC} levels.
Note 8: Device jitter added to the input signal.

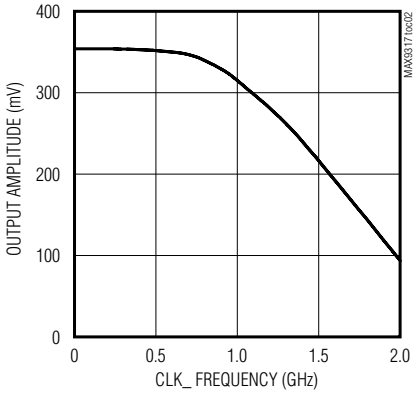
Typical Operating Characteristics

(MAX9317, V_{CC} = 2.5V, all outputs loaded with 100Ω ±1%, between Q_ and $\overline{Q}$_, f_{IN} = 1.0GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.)

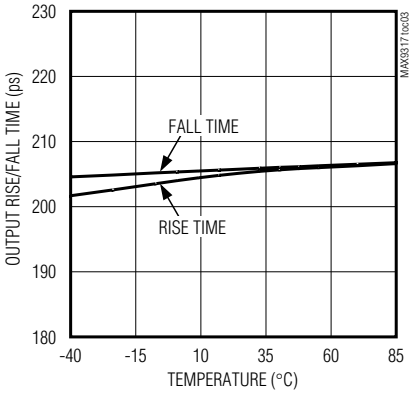
SUPPLY CURRENT vs. TEMPERATURE



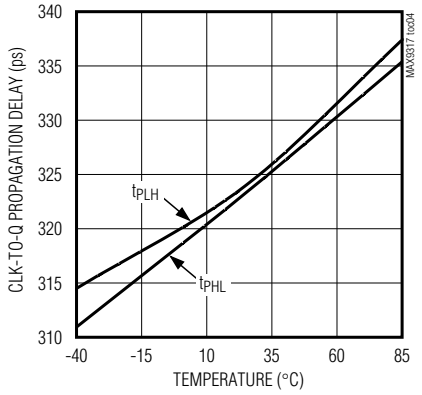
OUTPUT AMPLITUDE (V_{OH} - V_{OL}) vs. CLK_ FREQUENCY



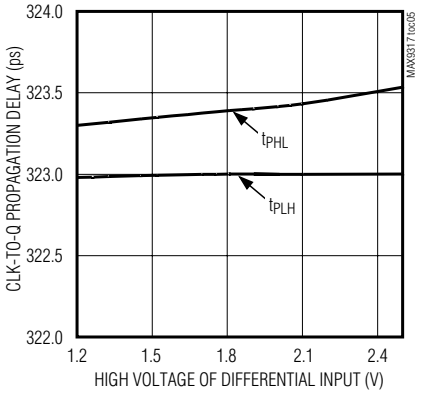
OUTPUT RISE/FALL TIME vs. TEMPERATURE



CLK-TO-Q PROPAGATION DELAY vs. TEMPERATURE



CLK-TO-Q PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



Pin Description

PIN	NAME		FUNCTION
	MAX9317 MAX9317B	MAX9317A MAX9317C	
1, 8	GND	GND	Ground
2	N.C.	—	No Connection. Connect this pin to ground or leave floating.
	—	V_{TA}	CLKA Input Termination Voltage. This pin is connected to CLKA and $\overline{CLKA}$ through 50Ω termination resistors. Connect this pin to V_{CC} - 2V for an LVPECL input signal on CLKA or leave floating for an LVDS input signal.
3	CLKA	CLKA	Noninverting Differential Clock Input A
4	$\overline{CLKA}$	$\overline{CLKA}$	Inverting Differential Clock Input A
5	N.C.	—	No Connection. Connect this pin to ground or leave floating.
	—	V_{TB}	CLKB Input Termination Voltage. This pin is connected to CLKB and $\overline{CLKB}$ through 50Ω termination resistors. Connect this pin to V_{CC} - 2V for an LVPECL input signal on CLKB or leave floating for an LVDS input signal.
6	CLKB	CLKB	Noninverting Differential Clock Input B
7	$\overline{CLKB}$	$\overline{CLKB}$	Inverting Differential Clock Input B
9, 16, 25, 32	V_{CC}	V_{CC}	Positive Supply Voltage. Bypass each V_{CC} pin to ground with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device.
10	$\overline{QB4}$	$\overline{QB4}$	CLKB Inverting Differential Output 4. Terminate with 100Ω to QB4.
11	QB4	QB4	CLKB Noninverting Differential Output 4. Terminate with 100Ω to $\overline{QB4}$.
12	$\overline{QB3}$	$\overline{QB3}$	CLKB Inverting Differential Output 3. Terminate with 100Ω to QB3.
13	QB3	QB3	CLKB Noninverting Differential Output 3. Terminate with 100Ω to $\overline{QB3}$.
14	$\overline{QB2}$	$\overline{QB2}$	CLKB Inverting Differential Output 2. Terminate with 100Ω to QB2.
15	QB2	QB2	CLKB Noninverting Differential Output 2. Terminate with 100Ω to $\overline{QB2}$.
17	$\overline{QB1}$	$\overline{QB1}$	CLKB Inverting Differential Output 1. Terminate with 100Ω to QB1.
18	QB1	QB1	CLKB Noninverting Differential Output 1. Terminate with 100Ω to $\overline{QB1}$.
19	$\overline{QB0}$	$\overline{QB0}$	CLKB Inverting Differential Output 0. Terminate with 100Ω to QB0.
20	QB0	QB0	CLKB Noninverting Differential Output 0. Terminate with 100Ω to $\overline{QB0}$.
21	$\overline{QA4}$	$\overline{QA4}$	CLKA Inverting Differential Output 4. Terminate with 100Ω to QA4.
22	QA4	QA4	CLKA Noninverting Differential Output 4. Terminate with 100Ω to $\overline{QA4}$.
23	$\overline{QA3}$	$\overline{QA3}$	CLKA Inverting Differential Output 3. Terminate with 100Ω to QA3.
24	QA3	QA3	CLKA Noninverting Differential Output 3. Terminate with 100Ω to $\overline{QA3}$.
26	$\overline{QA2}$	$\overline{QA2}$	CLKA Inverting Differential Output 2. Terminate with 100Ω to QA2.
27	QA2	QA2	CLKA Noninverting Differential Output 2. Terminate with 100Ω to $\overline{QA2}$.
28	$\overline{QA1}$	$\overline{QA1}$	CLKA Inverting Differential Output 1. Terminate with 100Ω to QA1.
29	QA1	QA1	CLKA Noninverting Differential Output 1. Terminate with 100Ω to $\overline{QA1}$.
30	$\overline{QA0}$	$\overline{QA0}$	CLKA Inverting Differential Output 0. Terminate with 100Ω to QA0.
31	QA0	QA0	CLKA Noninverting Differential Output 0. Terminate with 100Ω to $\overline{QA0}$.
—	EP	EP	Exposed Pad. QFN package only. Internally connected to ground.

Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs

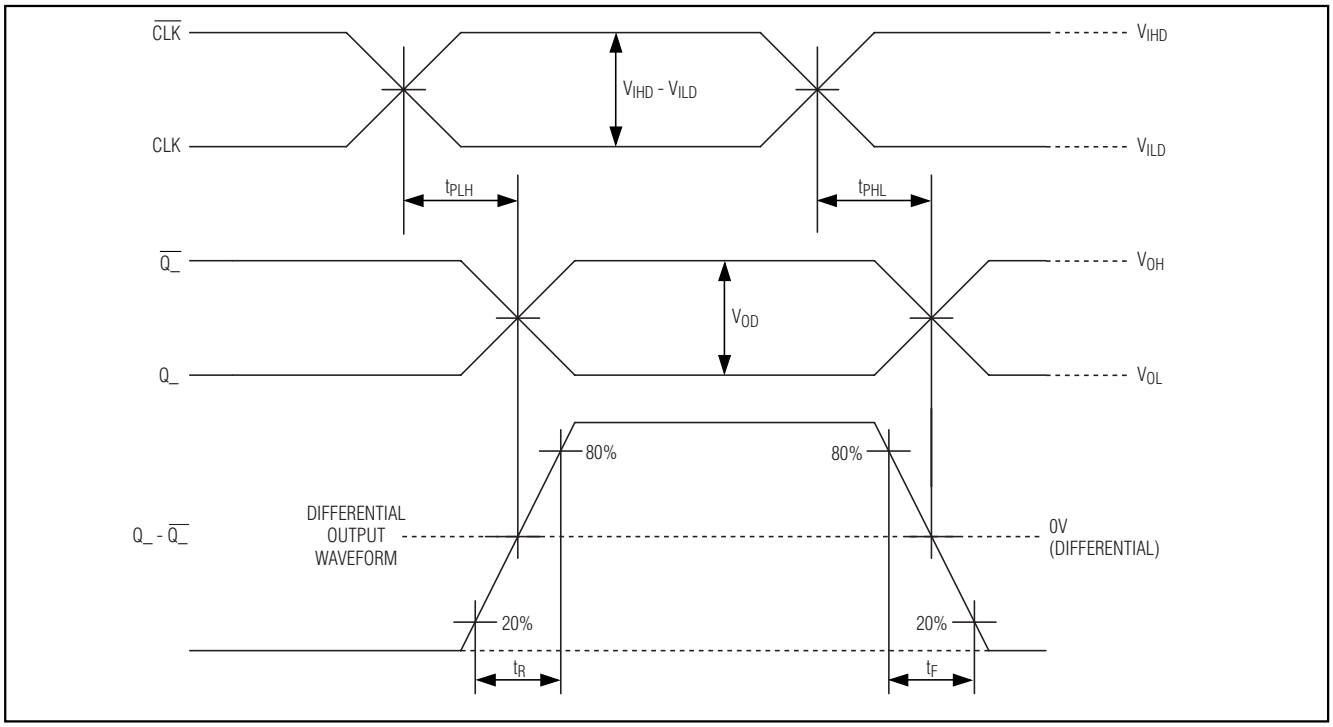


Figure 1. MAX9317 Timing Diagram

Detailed Description

The MAX9317 family of low-skew, 1-to-5 dual differential drivers are designed for clock or data distribution. Two independent 1-to-5 splitters accept a differential input signal and reproduce it on five separate differential LVDS outputs. The output drivers are guaranteed to operate at frequencies up to 1.0GHz with the LVDS output levels conforming to the EIA/TIA-644 standard.

The MAX9317/MAX9317A operate from a 2.375V to 2.625V power supply for use in 2.5V systems. The MAX9317B/MAX9317C operate from a 3.0V to 3.6V supply for 3.3V systems.

Differential LVPECL and LVDS Input

The MAX9317 family has two input differential pairs: CLKA and $\overline{CLKA}$, and CLKB and $\overline{CLKB}$. Each differential input pair can be configured or terminated independently. The inputs are designed to be driven by either LVPECL or LVDS signals with a maximum differential voltage of V_{CC} or 3.0V, whichever is less.

The MAX9317A/MAX9317C reduce external component count by having the input 50Ω termination resistors on chip. Configure the MAX9317A/MAX9317C to receive LVPECL signals by connecting $V_{T_}$ to V_{CC} - 2V (Figure 2(a)). Leaving the $V_{T_}$ input floating configures the

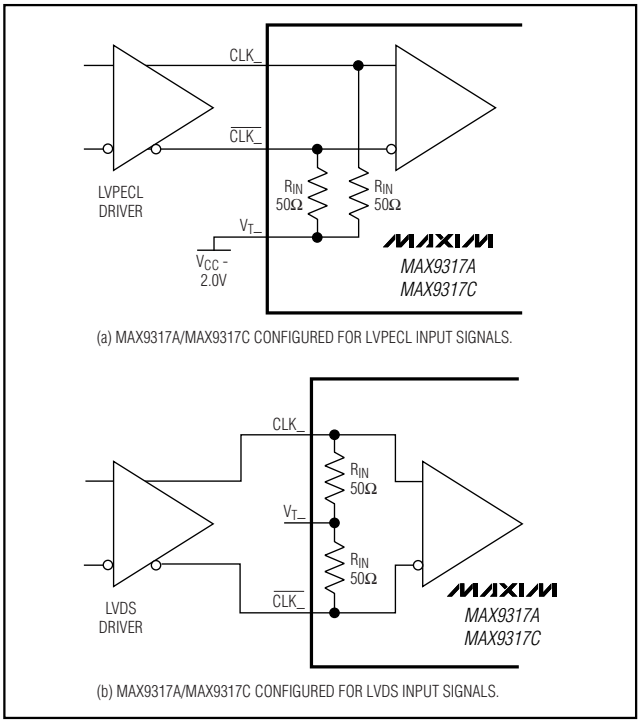


Figure 2. MAX9317A/MAX9317C Input Terminations

respective input with a differential 100Ω termination to receive LVDS signals (Figure 2(b)).

The MAX9317/MAX9317B accept LVPECL if the inputs are externally terminated with 50Ω resistors from CLKA and $\overline{CLKA}$ or CLKB and $\overline{CLKB}$ to V_{CC} - 2V. Alternatively, if the inputs are differentially terminated with 100Ω, they accept an LVDS input signal.

The LVDS input signal must adhere to the specifications given in the *Electrical Characteristics* table. Note that the signal must be at least 1.2V to be a valid logic HIGH.

Applications Information

Output Termination

Terminate the outputs with 100Ω across each differential pair (Q_ to $\overline{Q_}$). Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, observe the device's total thermal limits.

Power-Supply Bypassing

Bypass each V_{CC} pin to ground with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel and as close to the device as possible, with the 0.01µF capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance and reduce power-supply bounce with high-current transients.

Circuit Board Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Use 50Ω traces for CLK_, $\overline{CLK_}$, Q_, and $\overline{Q_}$. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity by keeping the differential traces close together.

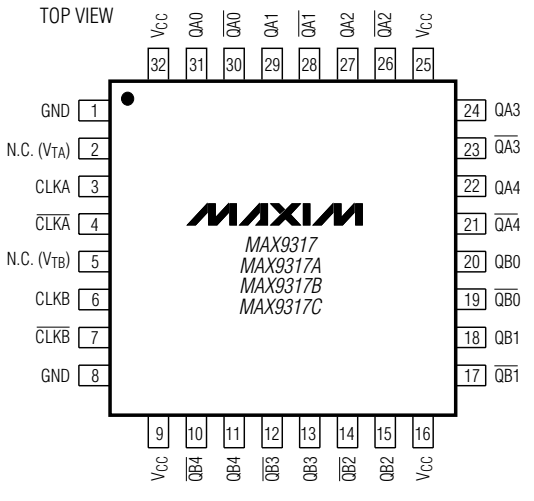
Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, and not using sharp corners or vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Chip Information

TRANSISTOR COUNT: 1119

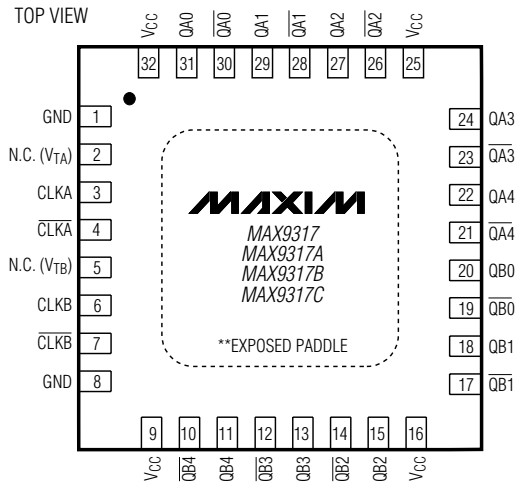
PROCESS: Bipolar

Pin Configurations



TQFP (7mm x 7mm)

( ) MAX9317A/MAX9317C.



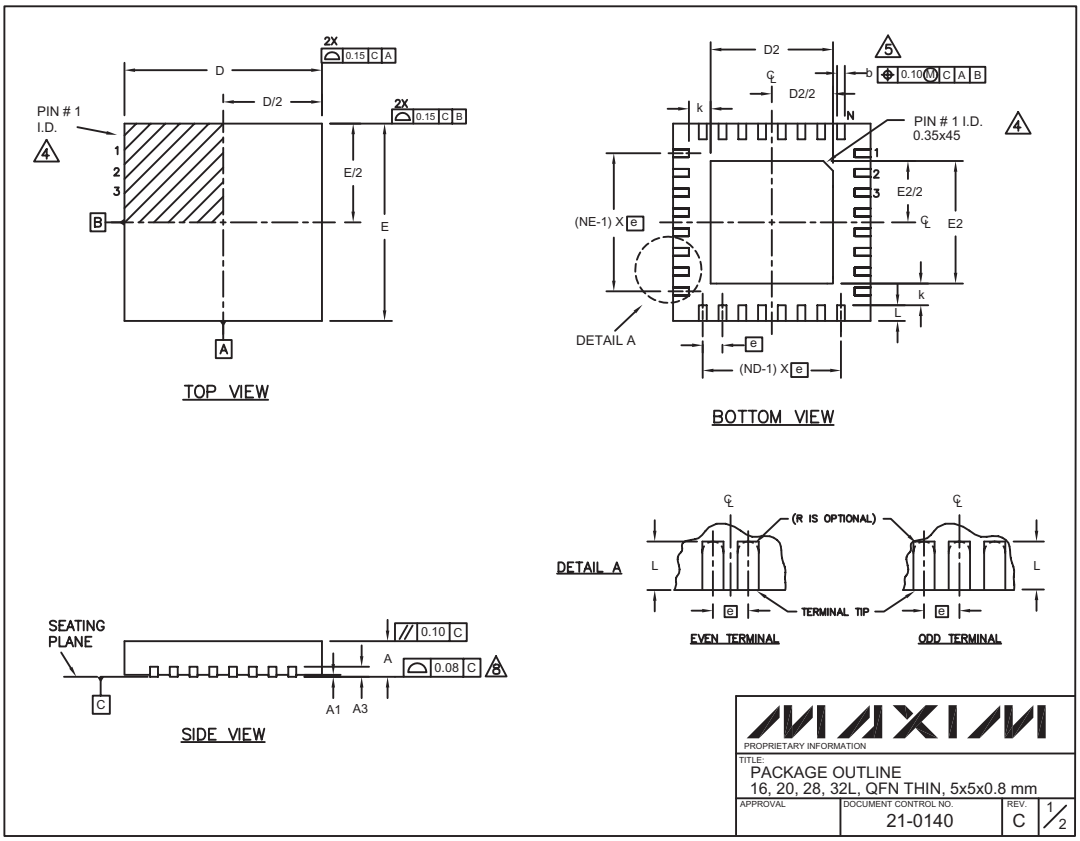
QFN-EP**

**EXPOSED PADDLE AND CORNER PINS ARE CONNECTED TO V_{EE}.

Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

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PROPRIETARY INFORMATION

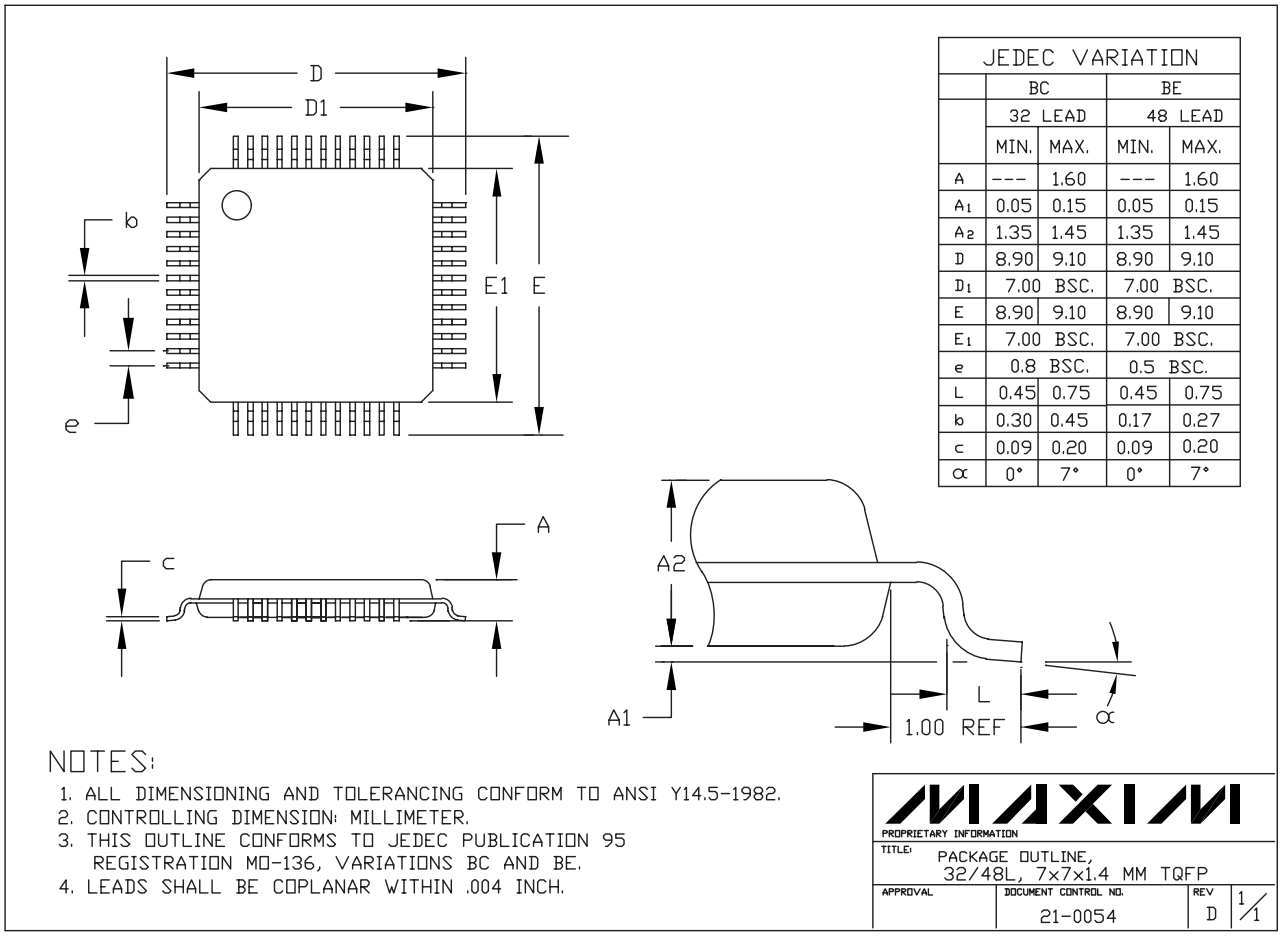
TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	C	2/2

Dual 1:5 Differential Clock Drivers with LVPECL Inputs and LVDS Outputs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

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PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	D	1/1

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